

 (a) (b)

**Adding AI to CMOS Image Sensors**: Edge computing using image sensors is expected to become increasingly important in the future, as edge data is fed into AI chips to process image data for face and object recognition. With that in mind, Sony researchers will describe a novel process that makes it possible to integrate an AI chip containing a built-in deep neural network (DNN), into the bottom wafer of a conventional two-wafer stacked CMOS image sensor. The wafer-on-wafer-on-wafer (WoWoW) process makes use of 6µm face-to-face and face-to-back Cu-Cu connections, and 6 µm through-silicon vias (TSVs). The researchers say the imaging characteristics of conventional 2-wafer-stacked image sensors are maintained, and the pixel density in the top chip was able to be increased to its theoretical limit. The device demonstrated high dynamic range, crucial for image quality, in both bright and dark environments.

* **The images above** are an architectural schematic and a SEM cross-sectional view of the 3-layer stacked image sensor, showing the integration of three wafers, designated as the top, middle, and bottom layers, through a WoWoW process.

**(Paper 14.4, “*Development of A Novel WoWoW Process for 1/1.3-inch 50 Megapixel Three-Wafer-Stacked CMOS Image Sensor with DNN Circuits*,” K. Shimizu et al, Sony)**